SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
Faculty of Engineering
Website: https://www.eng.nus.edu.sg/ece/

Area: Microelectronic Technologies & Devices

Host: Dr Li Yida

TOPIC	**:**	**All WSe_2 1T1R Resistive RAM Cell for Future Monolithic 3D Embedded Memory Integration**
SPEAKER	**:**	**Ms Maheswari Sivan** **Graduate student, ECE Dept, NUS**
DATE	**:**	**4 December 2019, Wednesday**
TIME	**:**	**9am to 10am**
VENUE	**:**	**E4-04-03, Engineering Block E4, Faculty of Engineering, NUS**

ABSTRACT

3-D monolithic integration of logic and memory has been the most sought after solution to surpass the Von-Neumann bottleneck, for which a low temperature processed material system becomes inevitable. Two dimensional materials, with their excellent electrical properties and low thermal budget are potential candidates. Here, we demonstrate a low temperature hybrid co-integration of one-transistor-one-resistor memory cell, comprising a surface functionalized 2-D WSe_2 *p*-FET, with a solution processed WSe_2 Resistive Random Access Memory. The employed plasma oxidation technique results in a low Schottky barrier height of 25 meV with a mobility of 230 $cm^2V^{-1}s^{-1}$, leading to a 100x performance enhanced WSe_2 *p*-FET, while the defective WSe_2 Resistive Random Access Memory exhibits a switching energy of 2.6 pJ per bit. Furthermore, guided by our device-circuit modelling, we propose vertically stacked channel FETs for high-density sub-0.01 μm^2 memory cells, offering a new beyond-Si solution to enable 3-D embedded memories for future computing systems.

BIOGRAPHY

Maheswari Sivan is currently pursuing her Ph.D degree in Electrical and Computer Engineering with specialization in microelectronics technology since 2017. Her research interest include exploring the opportunities and challenges of Two Dimensional Materials for advanced logic and memory applications.