SEMINAR ANNOUNCEMENT

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Area: Integrated Circuits & Embedded Systems

Host: Dr Lin Longyang

TOPIC	**:**	**Design considerations in low power hardware accelerators for convolutional neural networks**
SPEAKER	**:**	**Ms. Udari De Alwis** **Graduate student, ECE Dept, NUS**
DATE	**:**	**22 June 2020, Monday**
TIME	**:**	**5pm to 6pm**
WEBINAR	**:**	**URL Link : https://nus-sg.zoom.us/j/92882419882?pwd=bm1vSDZiekRvQnNTM05obkc4TytEdz09** **Meeting ID: 928 8241 9882** **Password: 877763**

ABSTRACT

With the development of the Internet of Things technology, more and more emphasis are being created on making edge devices smart and intelligent. The widespread use of visual sensors as edge nodes in IoT technology, has given rise to higher amounts of video data in the IoT data flows. With this context, video analysis in the edge nodes is an essential to have in future sensor nodes.

In the current research context, more and more computer vision tasks rely on the deep learning frameworks like Convolution Neural Networks (CNNs) due to the substantial performance improvements introduced by these algorithms. Yet the superior performance of CNN comes with a high computational complexity. The typical state of art CNNs comprises of millions of Multiplication and Accumulation (MAC) operations when it comes to inference. Low power hardware accelerators for convolutional neural networks accelerators focuses on reducing the computational cost as well as the memory access cost, enabling inferencing at the edge nodes where energy is a limited resource.

BIOGRAPHY

Udari De Alwis is currently a PhD student with the Department of Electrical and Computer Engineering, NUS. Her current research interest focuses on low power hardware accelerator architectures for deep neural networks.

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