SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
Faculty of Engineering
Website: https://www.eng.nus.edu.sg/ece/

Area: Integrated Circuits & Embedded Systems

Host: Assoc Prof Heng Chun Huat

TOPIC	**:**	**A 2.3-GHz 2.8-mW PI-Free Sampling ΔΣ PLL Achieving -110 dBc/Hz In-Band Phase Noise And 500-MHz FMCW Chirp**
SPEAKER	**:**	**Mr Su Hanyang** **Graduate Student, ECE Dept, NUS**
DATE	**:**	**Tuesday, 10 November 2020**
TIME	**:**	**12.00PM to 12.30PM**
WEBINAR	**:**	**Join Zoom Meeting** **https://nus-sg.zoom.us/j/81602170369?pwd=UzR5UmF1SXhBVFJZSGN5NGkxbmdkUT09**

ABSTRACT

A PI-free Fractional-N ΔΣ Sampling PLL (SPLL) has been proposed and implemented in 130-nm CMOS technology, which requires no phase interpolator (PI), digital-to-time converter (DTC) or background calibration. This PLL employs two linear slope generators (LSG) to produce linear waveforms, which are related to the VCO feedback phase. Then the reference directly samples the LSG outputs to obtain the phase error. Following which, a 3-bit DAC-based phase interpolating charge pump (PICP) is utilized to digitize the phase error before feeding it to loop filter. This enables the SPLL to achieve fractional-N ratio without any DTC or calibration. The superior linearity performance of the proposed DAC based PICP also leads to low fractional spur of -61.8 dBc. On-chip FMCW chirp generation is also included, which provides reconfigurable 500-MHz chirp with up to 25% chirp bandwidth to carrier frequency ratio. It consumes 2.8 mW from a 1.2 V supply and occupies an active area of about 0.4 mm2. With a 50-MHz crystal reference, the in-band phase noise is measured to be 110.7 dBc/Hz at 180 kHz offset.

BIOGRAPHY

Hanyang SU received the B.Eng. and M.Eng. degrees from Zhejiang University (ZJU), Hangzhou, China, in 2013 and 2016, respectively. He is now a Ph.D candidate of Faculty of Engineering, National University of Singapore. His research interests are in the field of analog and high-speed circuit design, including FMCW radar, PLL and ADC.