SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
Faculty of Engineering
Website: https://www.eng.nus.edu.sg/ece/

Area: Microelectronic Technologies & Devices

Host: Assoc Prof Aaron Danner

TOPIC	:	**Stochastic Cellular Automata Annealing (SCA) and its Non-Quantum Silicon Chip Implementation: Realizing Fully-Parallel Spin-Updates for Fully-Connected Spin Systems** ***[Author: Masato Motomura and Kazushi Kawamura]***
SPEAKER	:	**Prof Masato Motomura** **Tokyo Institute of Technology**
DATE	:	**Tuesday, 10 November 2020**
TIME	:	**10.00AM to 11.00AM**
WEBINAR	:	**Join Zoom Meeting** **https://nus-sg.zoom.us/j/6452107488?pwd=ckJXMTZBbzdJZ1pSOUd4VUJGSDdyQT09** **Meeting ID: 645 210 7488** **Password: 888888**

ABSTRACT

Stochastic cellular automata annealing (SCA) and its room-temperature non-quantum digital silicon chip implementation are presented. As opposed to simulated annealing, SCA allows fully parallel spin updates of fully connected spins by re-visiting and re-modeling the fundamental spin update dynamics of simulated annealing. A 65nm CMOS prototype chip, called STATICA, contains 512 fully-connected spins (0.25M interactions) on-chip, updating all the spins in one cycle (320MHz, 649mW). It is shown that STATICA outperforms all the existing annealing solutions.

BIOGRAPHY

Masato Motomura received the B.S., M.S., and Ph.D. degrees in electrical engineering from Kyoto University, Kyoto, Japan, in 1985, 1987, and 1996, respectively. In 1987, he joined the NEC central research laboratories, where he worked on various hardware architectures including string search engines, multi-threaded on-chip parallel processors, embedded DRAM field-programmable gate array (FPGA) hybrid systems, memory-based processors, and reconfigurable systems. From 2001 to 2008, he was with NEC Electronics where he led research and business development of dynamically reconfigurable processor (DRP) that he invented. He was also a visiting researcher at MIT laboratory for computer science from 1991 to 1992. From 2011 to 2019, he was a professor at Hokkaido University. He has been a Professor at Tokyo Institute of Technology, Japan, since 2019. His current research interests include reconfigurable and parallel architectures for deep neural networks, machine learning, annealing machines, and intelligent computing in general. Dr. Motomura is a member of IEICE, IPSJ, and EAJ. He was a recipient of the IEEE JSSC Annual Best Paper Award in 1992, the IPSJ Annual Best Paper Award in 1999, the IEICE Achievement Award in 2011, and the ISSCC Silkroad Award as the corresponding author in 2018, respectively.