SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
Faculty of Engineering
Website: https://www.eng.nus.edu.sg/ece/

Area: Integrated Circuits & Embedded Systems

Host: Assoc Prof Jerald Yoo

TOPIC	**:**	**Introduction of DRAM**
SPEAKER	**:**	**Mr Han WU** **Graduate Student, ECE Dept, NUS**
DATE	**:**	**Monday, 19 April 2021**
TIME	**:**	**10.00AM to 10.30AM**
WEBINAR	**:**	**Zoom Meeting link:** **https://nus-sg.zoom.us/j/2177921214?pwd=cFl1dVQxMCt4MG0vcEUxNVlSMEQwZz09** **Meeting ID: 217 792 1214** **Password: 20210428**

ABSTRACT

As pointed out by Turing Laureate David Patterson, the division of the semiconductor industry into microprocessor and memory camps has many advantages such as faster microprocessors and denser memory transistors. However, at the same time, the split into two camps has its disadvantage as well. The development of semiconductor industry shows that while microprocessor performance has been improving at a rate of 60% per year, the access time to DRAM (Dynamic Random Access Memory) has been improving at less than 10% per year. Despite heroic efforts by architects, compiler writers, and applications developers, memory accessing speed limits more applications today than it did in the past. In this seminar, the brief history of DRAM will be introduced and its operation such as write, read, refresh will also be illustrated. Furthermore, the DRAM category and speed trend will be discussed to enlighten advanced DRAM development.

BIOGRAPHY

Mr. Han WU received his B.Eng. degree in Electronic Science and Technology, M.E. degree in Microelectronics and Solid-State Electronics from College of Opto-electronic Engineering, Chongqing University, Chongqing, China, in 2013 and 2016. He is a Ph.D. student in the Electrical and Computer Engineering Dept., National University of Singapore since 2017. His research focuses on energy-efficient high-speed links, ultra-low power system-on-chip design, MEMS sensor interface circuit design, etc.