

SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
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Area: Integrated Circuits & Embedded Systems

Host: Assoc Prof Jerald Yoo

IEEE Solid-State Circuit Society (SSCS) Distinguished Lecture

TOPIC	:	On-Chip Physical Attack Protection Circuits for Hardware Security
SPEAKER	:	Prof. Makoto Nagata Kobe University, Japan
DATE	:	Monday, 6 September 2021
TIME	:	4.00PM to 5.00PM
WEBINAR	:	Join Zoom Meeting https://nus-sg.zoom.us/j/89729552123?pwd=alpieURBd2R6Y0x4dzd6aVp5dDJ2UT09 Meeting ID: 897 2955 2123 Passcode: 954822

ABSTRACT

Hardware security, application of modern digital cryptography and authentication technologies for protecting information in electronics, involves analog functionality to avoid physical threats in operation fields. This presentation provides an overview with historical aspects of on-chip physical attack protection circuits and assembly structures for the detection and disablement of malicious attempts on cryptographic devices. Design examples to combat passive and active side channel attacks as well as hardware Trojans are discussed and demonstrated with test vehicles.

BIOGRAPHY



Makoto Nagata received the B.S. and M.S. degrees in physics from Gakushuin University, Tokyo, in 1991 and 1993, respectively, and a Ph.D. in electronics engineering from Hiroshima University, Hiroshima, in 2001. He was a research associate at Hiroshima University from 1994 to 2002, an associate professor at Kobe University from 2002 to 2009 and promoted to a full professor in 2009. He is currently a professor of the graduate school of science, technology and innovation, Kobe University, Kobe, Japan. He is a senior member of IEICE and IEEE.

His research interests include design techniques targeting high-performance mixed analog, RF and digital VLSI systems with particular emphasis on power/signal/substrate integrity and electromagnetic compatibility, testing and diagnosis, three-dimensional system integration, as well as their applications for hardware security and safety.

Dr. Nagata has been a member of a variety of technical program committees of international conferences such as the Symposium on VLSI Circuits (2002-2009), Custom Integrated Circuits Conference (2007-2009), Asian Solid-State Circuits Conference (2005-2009), International Solid-State Circuits Conference (2014-2017), European Solid-State Circuits Conference (2020-) and many others. He is chairing the Technology Directions subcommittee for International Solid-State Circuits Conference (2018-present). He is also serving as SSCS AdCom member (2020-). He is currently an associate editor for IEEE Transactions on VLSI Systems (2015-present). He was a technical program chair (2010-2011), a symposium chair (2012-2013) and an executive committee member (2014-2015) for the Symposium on VLSI circuits, and also a chair for IEEE SSCS Kansai Chapter (2017-2018).