SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF DESIGN AND ENGINEERING
Website: https://cde.nus.edu.sg/ece

Area: Integrated Circuits & Embedded Systems

Host: Associate Professor Jerald Yoo

IEEE Solid-State Circuit Society (SSCS) Distinguished Lecture

TOPIC	:	**Integrated Security Interface Against Cyber-Physical Attacks**
SPEAKER	:	**Professor Noriyuki Miura** **Osaka University, Japan**
DATE	:	**Tuesday, 13 December 2022**
TIME	:	**2:00PM to 3:00PM**
VENUE	:	**E5-02-32** **NUS College of Design and Engineering, NUS**

ABSTRACT

The continuous growth in computing technology emerges various advanced information services today. The information managed in such services is becoming increasingly critical and hence valuable for malicious attackers. In order to steal, destroy, or manipulate such information in a cyber domain, the attackers exploit security holes in a physical domain computing entity i.e. IC hardware. These so-called cyber-physical attacks are currently one of the most serious security threats in realizing future advanced information society where the information security is the-root-of-trust of all the critical services such as autonomous driving, drone guard, and robot nursing. This lecture will cover several key countermeasures namely integrated security interface against the cyber-physical attacks, including 1) power/EM side-channel, 2) EM/laser fault-injection, 3) chip-package-board hardware counterfeiting, 4) sensor spoofing attacks, and 5) future perspectives on the information security in the next-generation society.

BIOGRAPHY

Noriyuki Miura received the B.S., M.S., and Ph.D. degrees in electrical engineering all from Keio University, Yokohama, Japan, in 2003, 2005, and 2007 respectively. From 2005 to 2008, he was a JSPS Research Fellow and since 2007 an Assistant Professor with Keio University, where he developed wireless interconnect technology for 3D integration. In 2012, he moved to Kobe University, Kobe, Japan, and became a Professor at Osaka University, Suita, Japan in 2020. Also, he was concurrently appointed as a JST PRESTO researcher, and now working on hardware security/safety and next-generation heterogeneous computing systems. Dr. Miura is currently serving as a Technical Program Committee (TPC) Member for A-SSCC and Symposium on VLSI Circuits. He served as the TPC Vice Chair of 2015 A-SSCC. He was a recipient of the Top ISSCC Paper Contributors 2004-2013, the IACR CHES Best Paper Award in 2014.

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