SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF DESIGN AND ENGINEERING
Website: https://cde.nus.edu.sg/ece

Area: Microelectronic Technologies & Devices

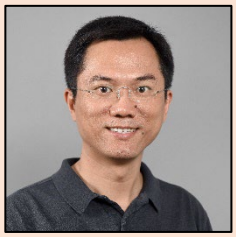
Host: Dr Fong Xuanyao

TOPIC	:	**Reliable In-memory Computing with Unreliable Devices and Circuits**
SPEAKER	:	**Professor Yu Cao, Kevin** **Electrical Engineering, Arizona State University, Tempe, Arizona**
DATE	:	**Wednesday, 21 December 2022**
TIME	:	**2.00PM to 3.30PM**
VENUE	:	~~**E5-03-20 Seminar Room**~~ ~~**NUS College of Design and Engineering, NUS**~~ **[Virtual Seminar]** **Join Zoom Meeting** **https://nus-sg.zoom.us/j/89849604143?pwd=M2g2Q3dEN2tVc1gwQ1JVUUZybjBxUT09** **Meeting ID: 898 4960 4143** **Password: 213109**

ABSTRACT

With the ever-increasing demand of AI algorithms and high-definition sensors, Contemporary microprocessor design is facing tremendous challenges in memory bandwidth, processing speed and power consumption. Leveraging the advances in device technology and design techniques, in-memory computing (IMC) embeds analog deep-learning operations in the memory array, achieving massively parallel computing with high storage density. On the other side, its performance is still limited by device non-idealities, circuit precision, on-chip interconnection, and algorithm properties. In this talk, we will first review the state-of-the-art IMC design techniques, such as those based on resistive random-access memory (RRAM) and SRAM. Then based on statistical data from a fully integrated 65nm CMOS/RRAM test chip, we will illustrate the bottlenecks of current IMC system, including RRAM variations, the stability of machine learning models, peripheral circuits and interconnection. They interact with each other, limiting the inference accuracy and system energy-delay product (EDP). To efficiently explore design space, we will present a newly developed benchmark simulator, SIAM, which integrates device, circuit, architecture, network-on-chip (NoC), network-onpackage (NoP) and DRAM access models to address the bottlenecks in data movement and robustness. Furthermore, we will demonstrate two methods to recover the accuracy loss: training for model stability before mapping to the hardware, and a hybrid SRAM/RRAM architecture for post-mapping recovery. These methods are applied to various datasets as well as a 65nm SRAM/RRAM test chip, helping shed light on future IMC research focus.

BIOGRAPHY



Yu Cao received the B.S. degree in physics from Peking University in 1996. He received the M.A. degree in biophysics and the Ph.D. degree in electrical engineering from University of California, Berkeley, in 1999 and 2002, respectively. He is now a Professor of Electrical Engineering at Arizona State University, Tempe, Arizona. He has published numerous articles and two books on nano-CMOS modeling and physical design. His research interests include neural-inspired computing, hardware design for on-chip learning, and reliable integration of nanoelectronics. Dr. Cao is a Distinguished Lecturer of the IEEE Circuits and Systems Society. He was a recipient of the 2020 Intel Outstanding Researcher Award, the 2009 ACM SIGDA Outstanding New Faculty Award, the 2006 NSF CAREER Award, the 2006 and 2007 IBM Faculty Award, and five Best Paper Awards. He is a Fellow of the IEEE.