We are a young fabless IC design company, headquartered in China. In Singapore site, our R&D team works on WiFi SoC products. We are looking for talented engineers to join our Design Verification team.

Read on for detailed job description. Interested candidates can send his/her resume to Xiaolei.Chen@supremicro.com

Design Verification Engineer, Senior

Responsibilities include:

- Actively understand Design under Test (DUT);
- Define and peer-review test plan;
- Write test patterns as per defined test plan;
- Execute test patterns, actively debugging RTL simulation issues;
- Execute regression of test patterns;
- Collect and actively improve RTL code coverage;
- Document test patterns, and write sign off report;
- Provide help and guidance to junior members in team;

Required qualifications:

- Bachelor or Master degree, majoring Electrical or Computer Engineering;
- 3~5 years working experiences as either Designer or Verification Engineer;
- Experienced with logic design, using hardware description language Verilog or SystemVerilog;
- Experienced with UVM;
- Experienced with RTL simulation and debugging, using tools from any of the following vendors: Synopsys, Cadence, or Mentor;
- Experienced with Linux scripting (eg, Bash, C Shell, Perl, or Python)
- Good English communication skills;
- Basic knowledge of version control system (SVN for example);
- Self-motivated, self-disciplined and responsible;

Possessing any of the following will be advantage:

- Experienced with ARM CPU based digital system;
- Experienced with C programming;
- Experienced with low power simulation, using UPF;
- Experienced with gate level simulation;
- Experienced with design prototyping using FPGAs;
- Able to speak or read Chinese language;

Design Verification Engineer (Junior level)

Responsibilities include:

- Actively understand Design under Test (DUT);
- Define test plan with help and guidance from seniors;
- Write test patterns as per defined test plan;

Aug 2022

- Execute test patterns, actively debugging RTL simulation issues;
- Document test patterns, and write sign off report;

Required qualifications:

- Bachelor's degree, majoring Electrical or Computer Engineering;
- Experienced with logic design, using hardware description language Verilog or SystemVerilog;
- Experienced with RTL simulation and debugging, using tools from any of the following vendors: Synopsys, Cadence, or Mentor;
- Good English communication skills;
- Basic knowledge of version control system (SVN for example);
- Self-disciplined and responsible;

Possessing any of the following will be advantage:

- Experienced with UVM;
- Experienced with ARM CPU based digital system;
- Experienced with C programming;
- Experienced with Linux scripting (eg, Bash, C Shell, Perl, or Python)