***SEMINAR ANNOUNCEMENT***

**DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING**
**COLLEGE OF DESIGN AND ENGINEERING**
Website: https://cde.nus.edu.sg/ece

***Area: Microelectronic Technologies & Devices***

***Host: Dr. Han Kaizhen***

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| **TOPIC** | : | **CMOS Process Compatible InGaAs HEMTs on 200 mm Si Substrate** |
| **SPEAKER** | : | **Mr. Wang Chengkuan**<br>**Graduate Student, ECE Dept, NUS** |
| **DATE** | : | **Thursday, 30 March 2023** |
| **TIME** | : | **3.00PM to 4.00PM** |
| **VENUE** | : | **Join Zoom Meeting:**<br>**https://nus-sg.zoom.us/j/81163318317?pwd=RVB3RmhnOHd6b3c1Q3JXY1dZNjVjdz09**<br><br>**Meeting ID: 811 6331 8317**<br>**Passcode: 619625** |

## ABSTRACT

In wireless communication, with 5G and 6G as the next generation, there is a push towards higher operating frequencies, moving from the congested sub-6 GHz bands towards mm-wave bands (and beyond). To enable the next-generation RF front-end modules beyond 5G, CMOS compatible III-V-on-Si technology is one of the most promising paths. The major target is to achieve the co-integration of front-end components (such as power amplifiers and switches) with other CMOS-based circuits (such as control circuitry or transceiver technology) to reduce cost and enable new hybrid circuit topologies to address performance and efficiency. These targets require electronic systems which can offer low noise, high speed, and high signal power, i.e., the best of all material systems (Si, InGaAs, and GaN etc.) in a single package. Integration of InGaAs HEMTs and Si CMOS on large-area silicon substrates holds great promise to cater to the needs of beyond 5G technology owing to the extremely high electron mobility and bandgap engineering of InGaAs material systems and the mature Si platform. With the advances of epitaxial growth technology, the InGaAs HEMT heterostructure has been realized in a large diameter (200 mm) Si substrate which provides the possibility of fabricating devices on larger size and lower cost substrates with Si CMOS using CMOS-compatible processes. The CMOS-compatible processes bring the opportunity for on-chip integration of III-V devices with Si-integrated circuits (ICs). In this article, we have demonstrated In0.4Ga0.6As Schottky HEMTs on a 200 mm silicon substrate fabricated using CMOS-compatible processes for the first time, featuring planar device isolation using Argon ion implant and thermally stable device operation up to 400 °C.

## BIOGRAPHY

Wang Chengkuan is a PhD student at the Department of Electrical and Computer Engineering, National University of Singapore, advised by Prof. Gong Xiao. His research interest covers microelectronic devices. At present, he has been doing research about InGaAs HEMT devices on Si and IGZO Thin Film Transistors.

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