***SEMINAR ANNOUNCEMENT***

**DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING**
**COLLEGE OF DESIGN AND ENGINEERING**
Website: https://cde.nus.edu.sg/ece

***Area: Integrated Circuits & Embedded Systems***

***Host: Dr. Karim Ali Ahmed***

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| **TOPIC** | : | **Energy-efficient SAR ADC with Comparator Offset-Injection Assisted SAR Search and Inter-Sample Power-Gating** |
| **SPEAKER** | : | **Mr. Japesh Vohra**<br>**Graduate Student, ECE Dept, NUS** |
| **DATE** | : | **Friday, 14 April 2023** |
| **TIME** | : | **2:30PM to 3:00PM** |
| **VENUE** | : | **Join Zoom meeting:**<br>**https://nus-sg.zoom.us/j/84021085739?pwd=Wlh0Wmh5SEErQ0RVZ2VoaTQwcWtwQT09**<br><br>**Meeting ID: 840 2108 5739**<br>**Passcode: 048402** |


**ABSTRACT**

With the increasing demand for Internet of Things (IoT) and edge devices, the successive approximation register (SAR) architecture has garnered considerable interest in analog-to-digital conversion applications, particularly due to its energy efficiency, compact size, and operational flexibility in terms of resolution and conversion speed. For low-to-mid resolution and low-to-mid conversion rate analog-to-digital converters (ADCs), SAR and its hybrid architectures have been popular choices, experiencing tremendous improvements in the past two decades, benefiting from both technology scaling and enhanced architectural designs. However, to counter the effects of mismatch-induced variations in capacitive DACs and comparators, SAR ADCs with resolutions above 10 bits ubiquitously employ either calibration circuits or redundancies. Since calibration circuits need to counter the effects of variations, they require a small range of tunability but with high accuracy. In this seminar, recent advancements in SAR ADCs, their limitations, and a proposed design to reuse calibration circuits to assist SAR conversion, as well as to relax mismatch limitations, will be discussed.


**BIOGRAPHY**

Japesh is pursuing his PhD degree with the Green IC group at NUS. He received his B.Tech. in Electrical Engineering from Indian Institute of Technology Ropar in the 2018 and worked at Samsung Research and Development Institute for one year as a Software Engineer before joining NUS. His research focuses on designing energy-efficient circuits for real-time systems. He is currently working on designing low-power hybrid SAR ADCs and low-power smart image sensors with in-pixel saliency detection.