

SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF DESIGN AND ENGINEERING

Website: <https://cde.nus.edu.sg/ece>

Area: Integrated Circuits & Embedded Systems

Host: Professor Alioto, Massimo Bruno

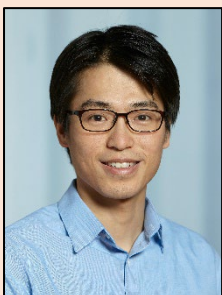
TOPIC	:	Energy Efficient Circuits Beyond what have been believed as the Fundamental Limits: Power Converter, Analog Interface and Frequency Generation
SPEAKER	:	Professor Taekwang Jang ETH Zurich, Switzerland
DATE	:	Monday, 19 June 2023
TIME	:	5.00PM to 6.00PM
VENUE	:	Block E3, E3-06-09 SEMINAR ROOM College of Design and Engineering, National University of Singapore

ABSTRACT

As circuit designers, we are entering an exciting new era where innovations in circuits are the key enablers for reshaping the future. With the emerging trends in Machine Learning, Internet-of-Everything, Brain-Machine Interfaces, Autonomous Driving, 6G Communication, Quantum Computing, and many more cutting-edge technologies, circuit designers are required to make drastic improvements in accuracy, speed, and energy efficiency.

Yet, as the CMOS circuit theories and design methodologies have been optimized and matured over the past five decades, we often encounter what so believed as the fundamental limit that confines the maximum achievable performance of a circuit. This may lead us to believe that no meaningful improvements can be made to it. However, such a limit is sometimes restricted to a specific topology or methodology, i.e., not so fundamental, the circuit may still have the potential to improve even by order of magnitude. As examples, I will explain our recent designs of 1) an on-chip high-power-density DC-DC converter 2) a noise-efficient sensor interface, and 3) a wide-bandwidth phase-locked loop that exceed previously believed limitations.

BIOGRAPHY



Taekwang Jang received his B.S. and M.S. in electrical engineering from KAIST, Korea, in 2006 and 2008, respectively. From 2008 to 2013, he worked at Samsung Electronics, focusing on mixed-signal circuit design, including analog and all-digital PLLs. In 2017, he received his Ph.D. from the University of Michigan; his dissertation was titled "Circuit and System Designs for Millimeter-Scale IoT and Wireless Neural Recording." After working as a post-doctoral research fellow, he joined the ETH Zürich in 2018 as an assistant professor and is leading the Energy-Efficient Circuits and IoT Systems group. He is also a member of the Competence Center for Rehabilitation Engineering and Science, and the chair of IEEE solid-state circuits society, Switzerland chapter.

His research focuses on circuits and systems for highly energy-constrained applications such as wireless sensor nodes and biomedical interfaces. Essential building blocks such as a sensor interface, energy harvester, power converter, communication transceiver, frequency synthesizer, and data converters are his primary interests. He holds 14 patents and has (co)authored more than 60 peer-reviewed conferences and journal articles. He is the recipient of the IEEE ISSCC 2021 and 2022 Jan Van Vessel Award for Outstanding European Paper, the IEEE ISSCC 2022 Outstanding Forum Speaker Award, and the 2009 IEEE CAS Guillemin-Cauer Best Paper Award. Since 2022, he has been a TPC member of the IEEE International Solid-State Circuits Conference (ISSCC), IMMD Subcommittee, and IEEE Asian Solid-State Circuits Conference (ASSCC), Analog Subcommittee. He is also an associate editor for the Journal of Solid-State Circuits (JSSC).

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