SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF DESIGN AND ENGINEERING
Website: https://cde.nus.edu.sg/ece

Area: Microelectronic Technologies & Devices

Host: Associate Professor Liang Gengchiau (Co-Supervisor)
Assistant Professor Gong Xiao (Supervisor)

TOPIC	:	**Probabilistic Bit Devices-based Ground State Logic for Probabilistic Computing**
SPEAKER	:	**Mr. He Yihan** **Graduate Student, ECE Dept, NUS**
DATE	:	**Tuesday, 27 June 2023**
TIME	:	**3.00PM to 3.30PM**
VENUE	:	**Join Zoom Meeting** **https://nus-sg.zoom.us/j/86242980204?pwd=L0NWQnVWcml5bE5kYmZybVRvcFdjdz09** **Meeting ID: 862 4298 0204** **Passcode: 151974**

ABSTRACT

In recent years, the investigation into emerging probabilistic nanodevices such as the stochastic magnetic tunnel junctions, has ignited a surge of research interest in probabilistic computing. These probabilistic nanodevices normally exhibit inherent stochasticity and rapid fluctuation capability reaching sub-nanosecond, which are nature-friendly to serve as the building block of promising nonconventional computing models. A representative example is that the ground state probabilistic logic (GSPL), specifically the logically synthesized multiplier based on GSPL offers prospective solutions to efficiently solve hard computational integer factorization characterized by large solution spaces.

The GSPL is an energy-based computational model, which is enabled by encoding the solution of the problem to be solved into the system's ground state. The configuration of GSPL is designed on the bidirectional connectivity of the Boltzmann machine. However, although most of the GSPL designs can map the correct solutions satisfying the truth table into the system's ground state, the energy landscape of the whole system is quite complicated when logically synthesizing basic GSPL gates to combinatorial GSPL circuits. As a result, resources-consuming annealing techniques such as simulated annealing and parallel annealing are unavoidable to improve performance. In this seminar, we present several design techniques including the high-energy-difference design scheme and multi-body interactions-based design scheme to simplify the energy landscape for both basic GSPL gates and logically synthesized GSPLs. The evidence from theoretic calculations and circuit simulations demonstrates that the proposed designs can introduce degeneracy in energy levels and improve the factorization accuracy of GSPL-based multipliers. In addition, we review the development of GSPL and discuss the potential studies for future studies.

BIOGRAPHY

Mr. He Yihan is currently pursuing his Ph.D. degree at the Department of Electrical and Computer Engineering, National University of Singapore, supervised by Assist Prof. Gong Xiao and Assoc Prof. Liang Gengchiau. His research mainly focuses on the physics-inspired computational model, probabilistic logic, and probabilistic devices for probabilistic computing.