SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF DESIGN AND ENGINEERING
Website: https://cde.nus.edu.sg/ece

Area: Integrated Circuits and Embedded Systems (ICES)

Host: Dr Hayate Okuhara

TOPIC	:	**Enabling low-power, low-bandwidth, low-wire count interfaces: The One-Wire system**
SPEAKER	:	**Mr Neelkamal Semwal** **Graduate Student, ECE Dept, NUS**
DATE	:	**Tuesday, 26 November 2024**
TIME	:	**10:00AM-11:00AM**
VENUE	:	**Join Zoom Meeting** **https://nus-sg.zoom.us/j/83323952782?pwd=OWHRjabZmsCc61bBk3m3tf6SxV9Zlf.1** **Meeting ID: 833 2395 2782** **Passcode: 035762**

ABSTRACT

The integration of deep sub-μW heterogeneous self-powered systems requires the support of off-chiplet routing of essential signals such as supplies, digital interfaces, timing, and power management. As opposed to single-chip designs, the complexity of off-chiplet routing conflicts with system cost, scalability (wire count increases with chiplet count between linearly and quadratically), substrate conformability and durability (degraded with more wires, e.g. in-textile), and substrate wire layer count and density limitations (e.g., stretchable). Thus, innovation in heterogeneous system integration is necessary to keep wire count minimal while distributing all necessary system-level signals, support reuse of chiplets from an existing collection (ecosystem), and keep power <<1 μW for sustained self-powered operation.

This work introduces a heterogeneous system architecture integrating chiplets with a minimal wireline interface of one wire, which simultaneously carries the regulated supply for all chiplets, voltage-mode downstream data transfers from hub to hosts, current-mode upstream data transfers, and distributed power management. Integration in a low-dimensional system is illustrated by a system-on-wire for human physical state monitoring where chiplets are integrated on a wire, using human body as return path (e.g., for in-textile use).

BIOGRAPHY

Mr. Neelkamal Semwal is currently a Master by Engineering student at NUS. His research interests include low-power, high-performance mixed signal circuits and architecture. He currently also works as a Research Engineer in the GreenIC research group at NUS led by Prof. Massimo Alioto. Neelkamal received his Bachelor of Technology (B.Tech) from National Institute of Technology (NIT) Silchar, India in 2019. He worked as a Senior Software Engineer at Ittiam Systems Pvt. Ltd., Bangalore, India from 2019 – 2022.