SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF DESIGN AND ENGINEERING
Website: https://cde.nus.edu.sg/ece

Area: Microelectronic Technologies and Devices (MTD)

Host: Prof Biplab Sikdar

TOPIC	:	**Heterogenous Technologies for Logic and Memory and their Ultra-dense 3D**
SPEAKER	:	**Dr Shengman Li** **Postdoctoral Scholar, Department of Electrical Engineering, Stanford University.**
DATE	:	**Friday, 2 May 2025**
TIME	:	**10:00AM-11:00AM**
VENUE	:	**Join Zoom Meeting** **https://nus-sg.zoom.us/j/8092137897?pwd=eXFwV0s2SW14VFBzYW5GVXJtdUtvQT09** **Meeting ID: 809 213 7897** **Passcode: 405792**

ABSTRACT

The energy and bandwidth of data movement between compute and memory chips across sparse interconnects pose critical energy and throughput challenges for abundant-data applications such as Artificial Intelligence/Machine Learning. Heterogeneous technologies for logic and memory and their integration into ultra-dense 3D architectures (e.g., with ≤100 nm 3D interconnect pitches) can potentially deliver 100× to 1,000× system-level energy-delay benefits over state-of-the-art for abundant-data applications. Innovations in beyond-silicon materials and devices form the basis for this approach. In this seminar, I will present two such examples: carbon nanotube field-effect transistors (CNFETs) for fast and low-energy digital logic and indium-tin-oxide field-effect transistors (ITO FETs) for high-density memory.

Parasitic resistance and capacitance in traditional CNFET structures were major obstacles to fast and energy-efficient CNFET logic circuits. My work on new doping techniques overcomes these challenges and enables the highest-performance CNFETs to date. The overall flow is compatible with large-scale fabrication in industrial facilities.

Amorphous ITO films were traditionally limited to transparent electrodes in large-area electronics such as displays and solar panels. I will present the first ultra-thin amorphous ITO FETs with ultra-low leakage in a 10 nm channel, enabling their application for high-density on-chip gain-cell memory.

Both CNFETs and ITO FETs enable ultra-dense monolithic 3D integration since they can be fabricated at low temperatures (<400 ˚C). I will present future directions for ultra-dense 3D integration of heterogeneous technologies including topics such as high-quality nanomaterial assembly and in-device thermal management.

BIOGRAPHY

Dr. Shengman Li is currently a Postdoctoral Scholar in the Department of Electrical Engineering at Stanford University. She earned her Ph.D. in Microelectronics and Solid-State Electronics (2020) and her bachelor's degree in Electronic Science and Technology (2015), both from Huazhong University of Science and Technology (HUST). Her work on energy-efficient oxide-semiconductor FETs (Nature Materials '19, IEDM '19, IEDM '20) earned her HUST's highest scholarship. From 2020 to 2022, she served as an Associate Professor in the Department of Materials Science and Engineering at Hunan University, China. In 2022, Dr. Li joined the research groups of Prof. Subhasish Mitra and Prof. H.-S. Philip Wong at Stanford University, where she has been collaborating closely with TSMC researchers on fast and low-energy digital logic using carbon nanotube FETs (CNFETs). Over the past three years, her research has consistently advanced the state of the art in CNFETs, including records for the highest-performance CNFETs to date (Symp. VLSI Tech.'23, IEDM '23, Symp. VLSI Tech.'24, IEDM '24).