SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF DESIGN AND ENGINEERING
Website: https://cde.nus.edu.sg/ece

Area: Microelectronic Technologies & Devices (MTD)

Host: Dr Zhou Zuopu

TOPIC	:	**Non-volatile SRAM based on back-end-of-line compatible technology enabling monolithic 3D integration**
SPEAKER	:	**Mr Xie Jiawei** **Graduate Student, ECE Dept, NUS**
DATE	:	**Thursday, 24 July 2025**
TIME	:	**10:00AM to 10:30AM**
VENUE	:	**Join Zoom Meeting** **https://nus-sg.zoom.us/j/5337559127?omn=88637564192** **Meeting ID: 533 755 9127**

ABSTRACT

In this seminar, we will introduce the first experimental demonstration of a Back-End-of-Line (BEOL)-compatible non-volatile SRAM (NV-SRAM), combining advanced ferroelectric capacitors for data retention and Indium Tin Oxide (ITO) field effect transistors (FETs) for increased integration density. Designed for seamless BEOL integration, the NV-SRAM enables monolithic 3D stacking above CMOS circuits, paving the way for ultra-high-density memory solutions with superior bandwidth. The discussion will cover key experimental outcomes, including non-volatile operation, energy efficiency, low-voltage performance, and scalability, highlighting the promising role of NV-SRAM technology in next-generation data-centric computing.

BIOGRAPHY

Xie Jiawei is currently pursuing his Ph.D. degree under the supervision of A/Prof. Gong Xiao with Department of Electrical and Computer Engineering (ECE), National University of Singapore (NUS). His current research interests are ITO FETs for memory and power applications.