SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF DESIGN AND ENGINEERING
Website: https://cde.nus.edu.sg/ece

Area: Microelectronic Technologies & Devices (MTD)

Host: Assoc Prof Zhu Chun Xiang & Prof Guo Yongxin

TOPIC	:	**Design for Manufacturing in RF CMOS Learning from a System-Level N-Varactor Failure**
SPEAKER	:	**Mr Duan Zhigang** **Graduate Student, ECE Dept, NUS**
DATE	:	**Monday, 20 July 2026**
TIME	:	**3:00PM-3:30PM**
VENUE	:	**Join Zoom Meeting** **https://nus-sg.zoom.us/j/82640637707?pwd=DFBlNamK0GicLl3oG6auKByTB3nE1z.1** **Meeting ID: 826 4063 7707** **Passcode: 612850**

ABSTRACT

RF CMOS chipsets are complex because they combine dense digital logic with many kinds of analog and mixed signal devices, such as LNAs, mixers, VCOs, PLLs and matching networks. This makes product yield highly sensitive to subtle interactions between circuit layout and backend process steps.

In this work, a low-power RF CMOS chipset showed severe, intermittent RX gain loss only at system-level test, while WAT, inline defects and RF bench measurements all appeared normal. System debug narrowed the issue to open N-varactor branches in the RX path, and physical failure analysis revealed Via1 opens and strong copper loss under large N-varactors, especially at higher capacitance.

The root cause was traced to charge stored on the varactor and its interconnect during Via1/M1 processing, which enhanced local electro-chemical copper erosion during later cleaning. Simple layout and PDK changes—adding redundant vias and providing early N-well-to-ground connections—were introduced to discharge this charge before aggressive cleans.

These measures removed the Via1 opens, restored RX gain and stabilized yield. The case highlights the need for RF DFM rules that explicitly consider charge-storage devices and BEOL cleaning interactions and offers a practical template for industry to prevent similar hidden failures in future RF SoCs.

BIOGRAPHY

Mr. Zhigang Duan is an EngD candidate in the Department of Electrical and Computer Engineering at NUS, supervised by Associate Prof. Zhu Chunxiang and Prof. Guo Yongxin. His research focuses on advanced semiconductor device process integration and system power delivery. He also serves as a senior department manager at a leading design house, responsible for process technology development.