SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF DESIGN AND ENGINEERING
Website: https://cde.nus.edu.sg/ece

Area: Microelectronic Technologies & Devices (MTD)

Host: Assoc Prof Zhu Chun Xiang & Prof Guo Yongxin

TOPIC	:	**Designing Clean Metal Etch and FOUP Handling for SRAM Yield: A Case Study on Via Bottom Void Failures**
SPEAKER	:	**Mr Duan Zhigang** **Graduate Student, ECE Dept, NUS**
DATE	:	**Wednesday, 22 July 2026**
TIME	:	**3:00PM-3:30PM**
VENUE	:	**Join Zoom Meeting** **https://nus-sg.zoom.us/j/83103448185?pwd=g4yik00d58ooOM3lXa4YryPfa8Qsnf.1** **Meeting ID: 831 0344 8185** **Passcode: 675035**

ABSTRACT

This work presents a case study on intermittent SRAM yield loss in a high-volume RF/CMOS product with otherwise normal WAT, inline defect and SPC data. Detailed failure analysis revealed via-bottom voids and severe copper thinning at the smallest Via1 contacts inside SRAM cells, while larger logic vias were unaffected. Correlation of yield with lot history, FOUP usage and queue time after metal etch pointed to a time-dependent contamination mechanism. CF-based polymers and airborne molecular contaminants from the metal-etch process were found to accumulate on FOUP surfaces and gradually outgas back onto wafers, attacking exposed via bottoms during extended queue time. To mitigate this “hidden” BEOL integration issue, we introduced two process changes: use of clean or fresh FOUPs immediately after critical metal-etch steps, and tighter queue-time control between metal etch and subsequent wet clean. Split-lot experiments confirmed that these measures significantly reduced via-bottom copper loss, eliminated SRAM opens and restored stable yield. The study highlights the importance of FOUP handling and time control as integral parts of clean metal-etch design, and provides practical guidelines for process and design engineers working on SRAM-rich advanced technologies.

BIOGRAPHY

Mr. Zhigang Duan is an EngD candidate in the Department of Electrical and Computer Engineering at NUS, supervised by Associate Prof. Zhu Chunxiang and Prof. Guo Yongxin. His research focuses on advanced semiconductor device process integration and system power delivery. He also serves as a senior department manager at a leading design house, responsible for process technology development.

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