

SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF DESIGN AND ENGINEERING

Website: <https://cde.nus.edu.sg/ece>

Area: Microelectronic Technologies & Devices (MTD)

Host: Assoc Prof Zhu Chun Xiang & Prof Guo Yongxin

TOPIC	:	A Novel Method to Manufacture Multi-Layer High Density Capacitor
SPEAKER	:	Mr Duan Zhigang Graduate Student, ECE Dept, NUS
DATE	:	Friday, 24 July 2026
TIME	:	3:00PM-3:30PM
VENUE	:	Join Zoom Meeting https://nus-sg.zoom.us/j/82669667058?pwd=SQNRaxOvluaRN5vf3NyDPTAJCH2ghg.1 Meeting ID: 826 6966 7058 Passcode: 962497

ABSTRACT

Modern AI xPU chipsets draw ever-increasing power from the system, making power integrity a primary design constraint rather than a secondary concern. To control PDN impedance and simultaneous-switching noise, decoupling must extend beyond PCB capacitors and on-die capacitance to include package-level capacitors positioned close to the die to reduce SI/PI issues. These package capacitors are required to deliver progressively higher capacitance density, lower profile and smaller footprint, which current industrial solutions—including CoWoS DTC/iCap and discrete embedded silicon capacitors—cannot fully satisfy for next-generation AI workloads. In this work, we focus specifically on the deep-trench-capacitor (DTC) process flow, identify its limitations in density, cost and mask scaling, and then propose a new multilayer trench-based process that avoids disruptive changes while significantly reducing mask count and cost for a given capacitance. The proposed flow is designed to increase effective capacitor density at lower cost and compatible thickness, and we also discuss the associated process.

BIOGRAPHY

Mr. Zhigang Duan is an EngD candidate in the Department of Electrical and Computer Engineering at NUS, supervised by Associate Prof. Zhu Chunxiang and Prof. Guo Yongxin. His research focuses on advanced semiconductor device process integration and system power delivery. He also serves as a senior department manager at a leading design house, responsible for process technology development.

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