SEMINAR ANNOUNCEMENT

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING
COLLEGE OF DESIGN AND ENGINEERING
Website: https://cde.nus.edu.sg/ece

Area: Integrated Circuits & Embedded Systems (ICES)

Host: Assoc Prof Heng Chun Huat

TOPIC	:	**High-Speed Receiver Targeting for Optical Transceiver Applications**
SPEAKER	:	**Mr Xiong Shijie** **Graduate Student, ECE Dept, NUS**
DATE	:	**Thursday, 12 November 2026**
TIME	:	**3:00PM-4:00PM**
VENUE	:	**E4-04-05 (E-Cube 1)**

ABSTRACT

With the rapid growth of AI clusters and cloud data centers, optical links are shifting from 50-Gb/s NRZ to 200-Gb/s and 400-Gb/s per-lane PAM-4 signaling, alongside dense multi-channel wavelength-division multiplexing (WDM) systems. Inside an optical transceiver, the analog receiver front-end relies on the transimpedance amplifier (TIA) to convert weak, high-speed photodetector currents into voltage signals for downstream mixed-signal or DSP equalizers.

This seminar reviews the architecture, design methods, and circuit bottlenecks of high-speed optical receiver analog ICs. We will begin by looking at how front-end topologies have developed over time. Specifically, we will cover passive termination, common-base and regulated-cascode (RGC) current buffers, distributed amplifiers, and inductively peaked shunt-feedback (SFB) TIAs. Through this review, we will examine how the transimpedance limit and high-frequency capacitive noise create a tight trade-off among gain, bandwidth, and sensitivity.

Next, we will discuss three practical challenges in modern optical receiver design. The first challenge is maintaining large-signal PAM-4 linearity across a wide input dynamic range without adding parasitic loading or triode distortion from standard automatic gain control (AGC) switches. The second is pushing the bandwidth beyond 100 GHz while avoiding the power wasted by idle dummy stages in pseudo-differential front-ends. The third is reducing shared-supply and substrate noise crosstalk in compact, low-voltage multi-channel WDM receivers.

Finally, to address these issues, we will share our recent circuit work on active-feedback linear gain control, coupled-inductor bandwidth extension, and feedforward supply-noise-canceling single-to-differential (S2D) conversion.

BIOGRAPHY

Xiong Shijie is currently pursuing the Ph.D. degree in the Department of Electrical and Computer Engineering, National University of Singapore (NUS), under the supervision of Assoc. Prof. Heng Chun Huat and Prof. Gao Yuan. His current research focuses on high-speed optical receiver front-ends, broadband linear transimpedance amplifiers (TIAs), and mixed-signal wireline/optical transceiver integrated circuits in advanced SiGe BiCMOS and FinFET CMOS technologies.

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