SSMC Dispatching Optimization

IE3100 System Design Project

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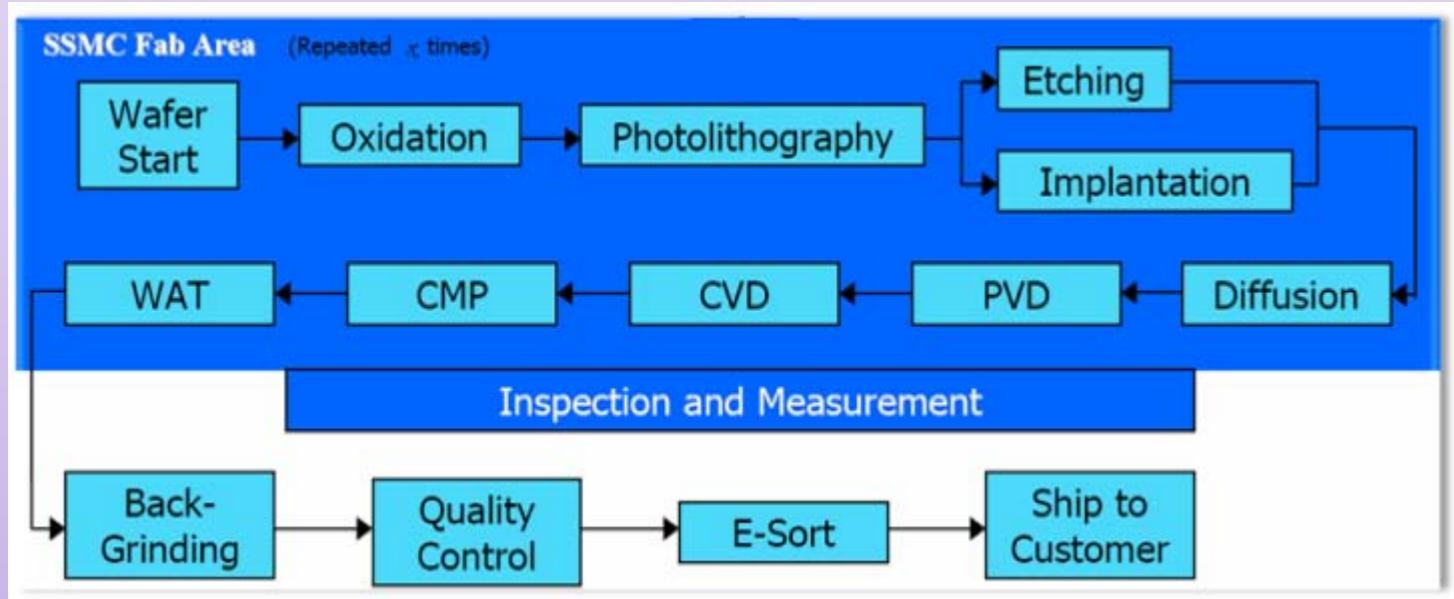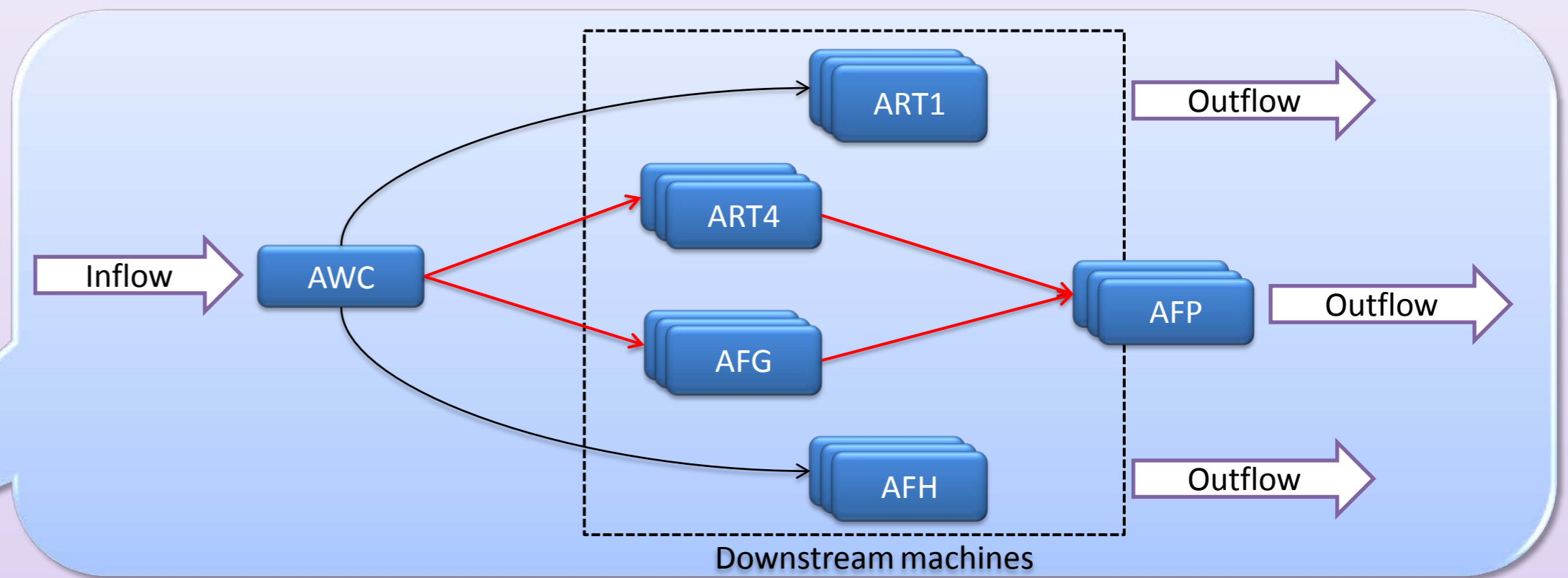ASST PROF NG SZU HUI

BACKGROUND

Systems on Silicon Manufacturing Co. Pte. Ltd (SSMC) is a world class semiconductor foundry which supplies chip products to a wide range of industries, by offering flexible and cost effective semiconductor fabrication solutions through the utilization of advanced sub-micron processes.

Basic Definition

Lot: One processing unit in the fabrication with maximum 25 wafers
Furnace and other downstream: Deposition of semi-conductor materials to the wafer surface

OBJECTIVES

Develop a *systematic algorithm* for dispatching wafers from wet bench to downstream machines to
➤Satisfy all constraints
➤Meet daily waferout target

Generation of loading priority at Wet Bench

PROBLEM DESCRIPTION

Terminologies and Constraints

Stage: set of steps each wafer go through to attain a desired characteristic
Technology: set of characteristics doped to each wafer according to customer's requirement
Recipe: set of instruction carried out by a machine on each wafer
DSP: A number that shows the urgency of a lot, considering all the following criteria
➤Priority type: Super Hot Lot (SHL), Hot Lot, Normal Lot
➤Critical Ratio: (Time to delivery)/(Remaining processing time)
➤OPQT: Maximum queuing time required by certain process steps
Batch Size: The number of wafers in one batch to be loaded into a certain machine
Stage target: The targeted amount of wafer lots to be processed by the end of day for each stage

Problem Description

Current dispatching process is established based on global rule to meet delivery:
Difficulty to manage tool output based on this global rule
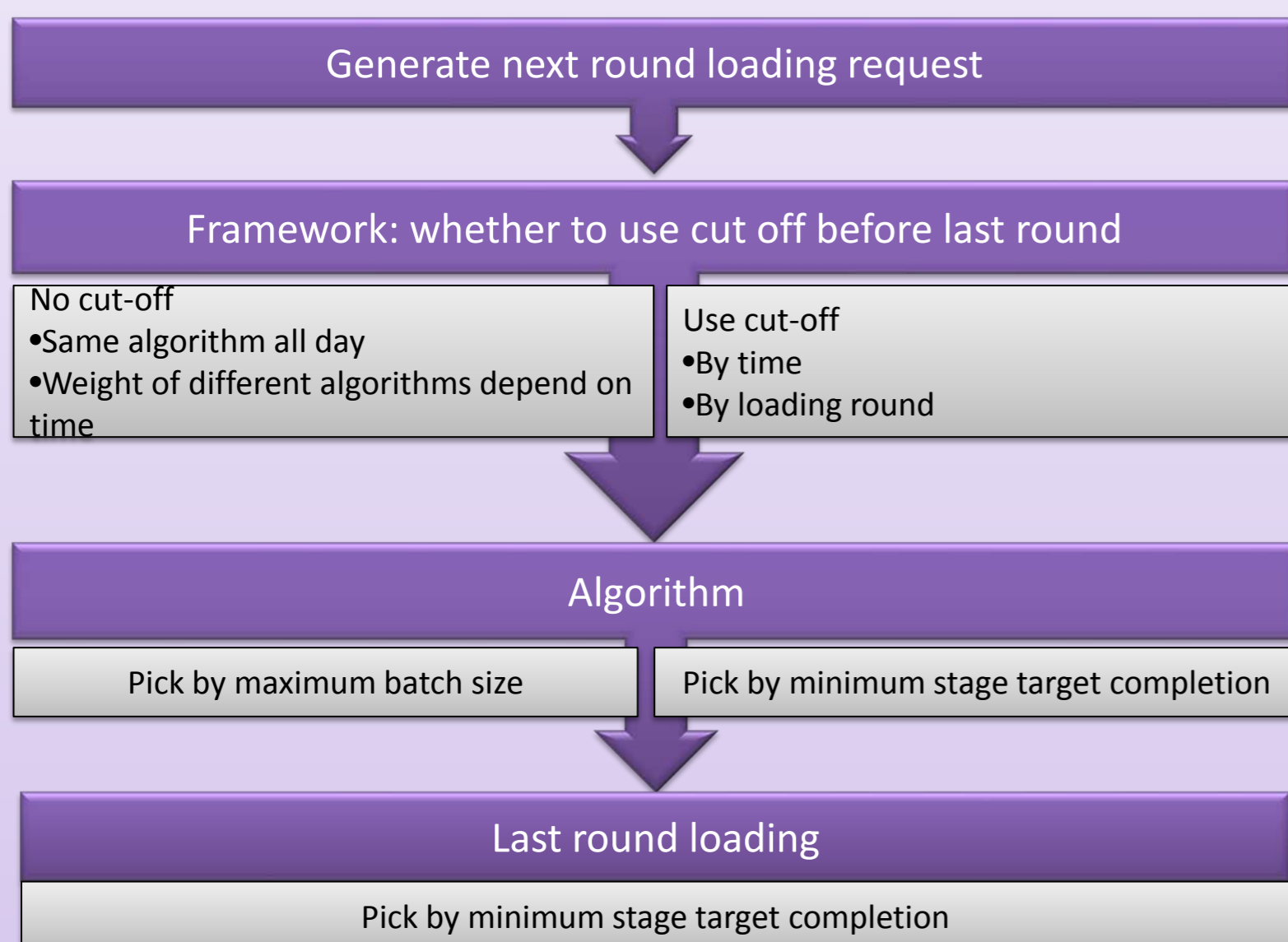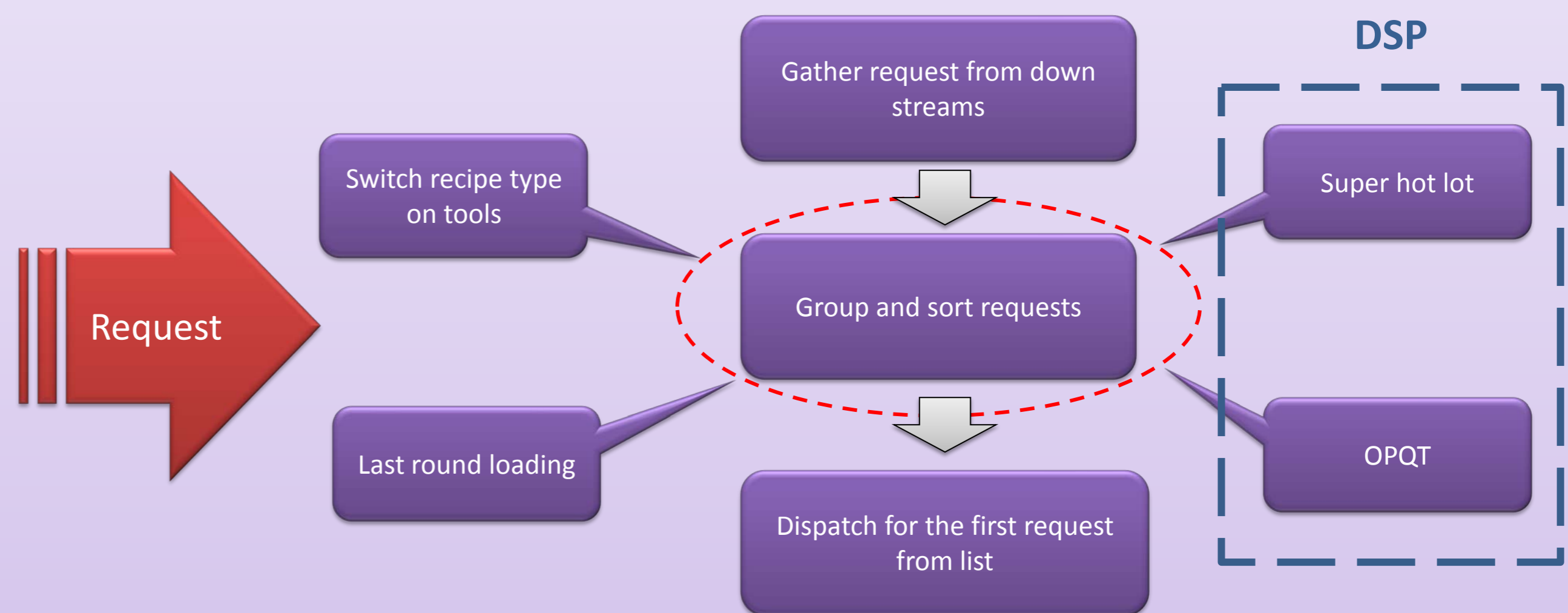Low adaptability to any changes

APPROACHES AND METHODOLOGY

Furnace: request generation

Wet bench: sort and dispatch the requests

Sorting algorithms: Earliest due date, minimum total tardiness, other heuristic rules.

To fully utilize the furnace capacity, a request should be sent to AWC after deciding the wafer recipe to be loaded next round. The request will be generated using the real time information available, such as the lots at AWC and Furnaces. Two basic sorting algorithm can be used: maximum-batch-size (MBS) and minimum-stage-target-completion (MSTC).
➤MBS algorithm: achieve higher machine efficiency
➤MSTC algorithm: balance the stage target completion among different stages
To achieve the best trade-off of machine utilization and stage target completion, different frameworks are proposed to use MBS algorithm and/or MSTC algorithm.

Recipe type at wet bench: Requests are grouped into long or short recipe request according to required processing time at wet bench.
DSP Priority: Super Hot Lot (SHL) is covered in DSP Priority. Lots with higher priority, by referring to DSP_Priority must be processed as soon as possible at each step. It jumps the queue in the request list.
OPQT: OPQT is the maximum queuing time at downstream tools. Hence, the lots are only processed when there is a request triggered (Controlled by dummy step).
Last Round Loading: Last round loading request should not be delayed in order to fulfill the daily stage target.

SIMULATION AND IMPLEMENTATION

We use Automod in simulation to evaluate the algorithms and select the best based on the performances.
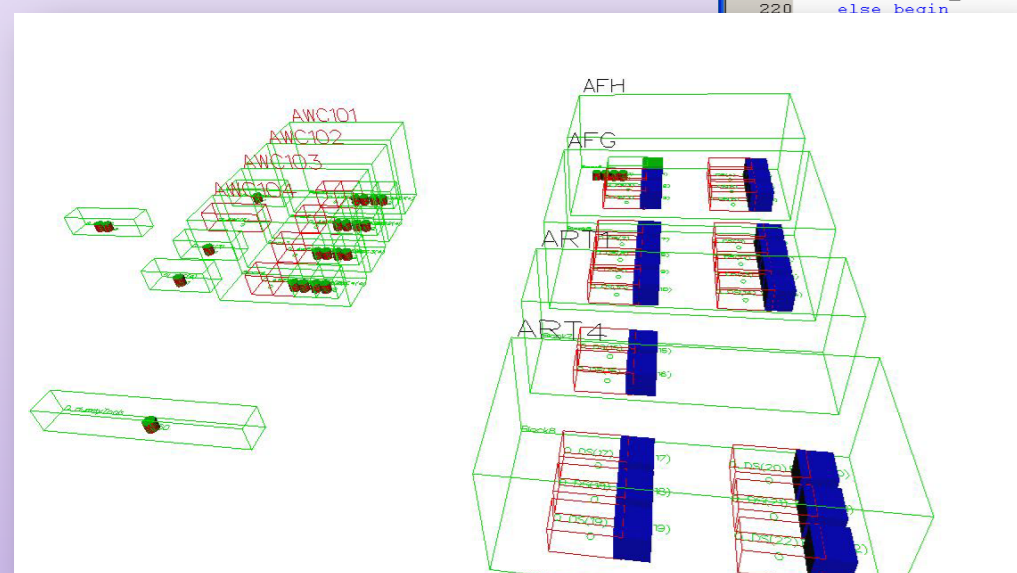
After the implementation of the algorithm, using the following two kinds of user interfaces makes dispatching process more systematic and efficient.

The wet bench MA should load the two lots shown at the top of list.

The downstream MA can see all the information and monitor the process.